# An Intel Perspective on Silicon Nanoelectronics

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# Outline

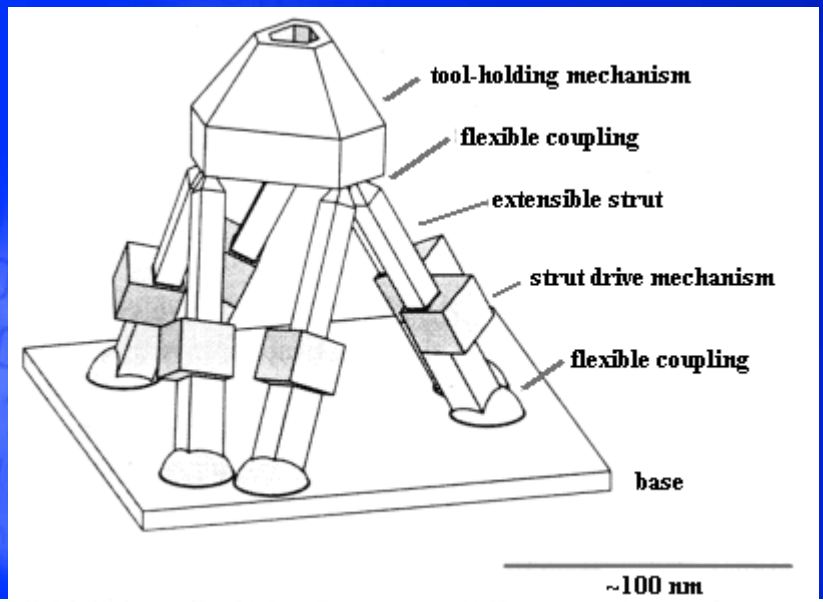
- What is Nanotechnology
- Intel's Current Nanotechnology and Scaling
- Future Scaling and Technologies
- Lessons from Nano Electronics for Others

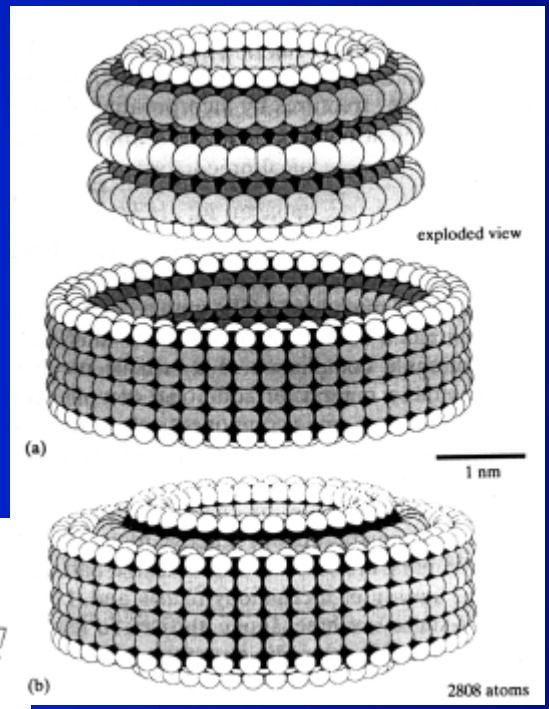
# Nanotechnology

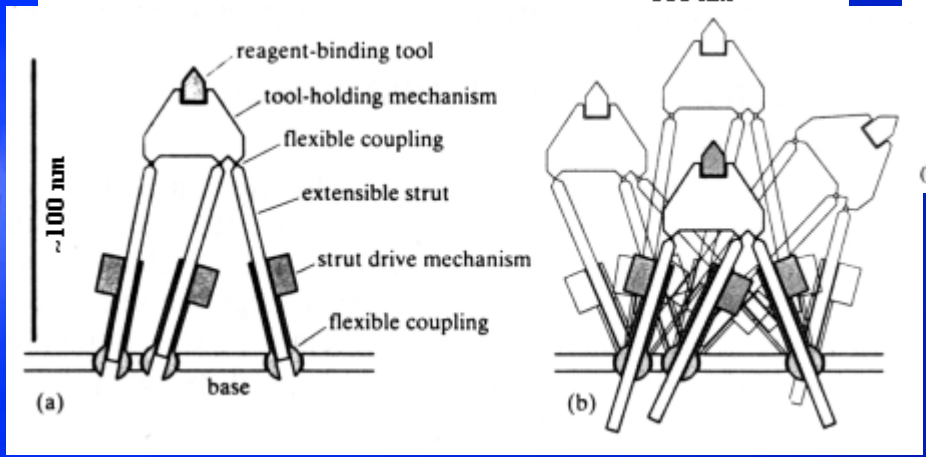
- Many companies, including Intel, are trying to understand the future impact of Nanotechnology on their business environment, their products, and their research priorities
- Intel can also look to the past impacts of Nanotechnology on its business and products

**Other Industries can learn from our experience**

# What is Nanotechnology?



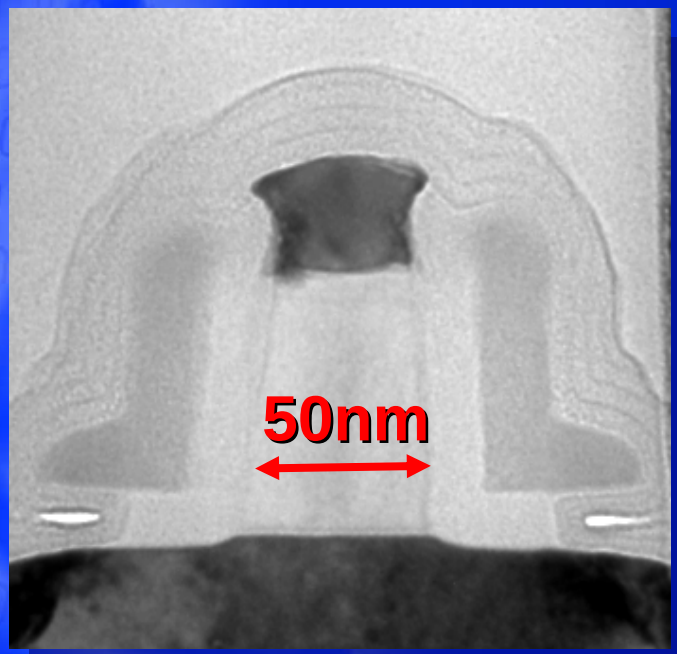




**K. Eric Drexler**

http://www.aeiveos.com/~bradbury/Authors/Engineering/Drexler-KE/index.html

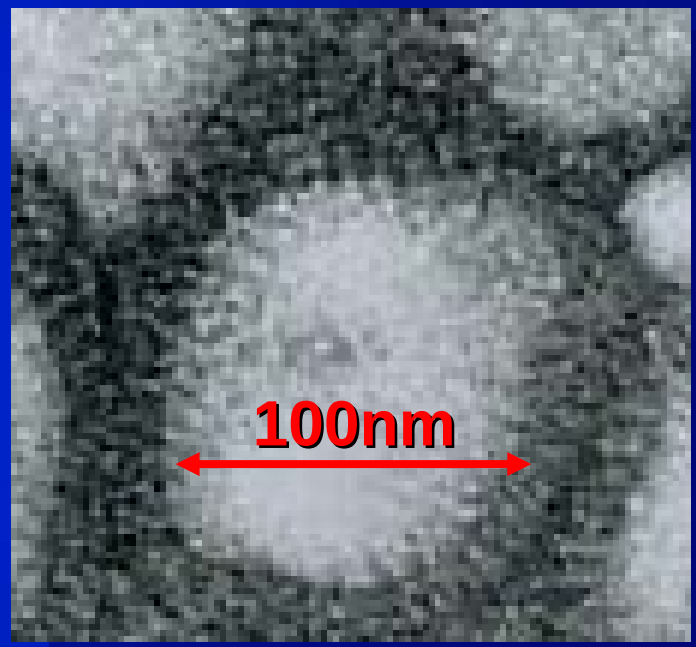
# Silicon Nanotechnology

*50 nm transistor dimension is ~2000x smaller than diameter of human hair*




**Transistor for 90nm Process**

**Source: Intel**




**Influenza virus**

**Source: CDC**

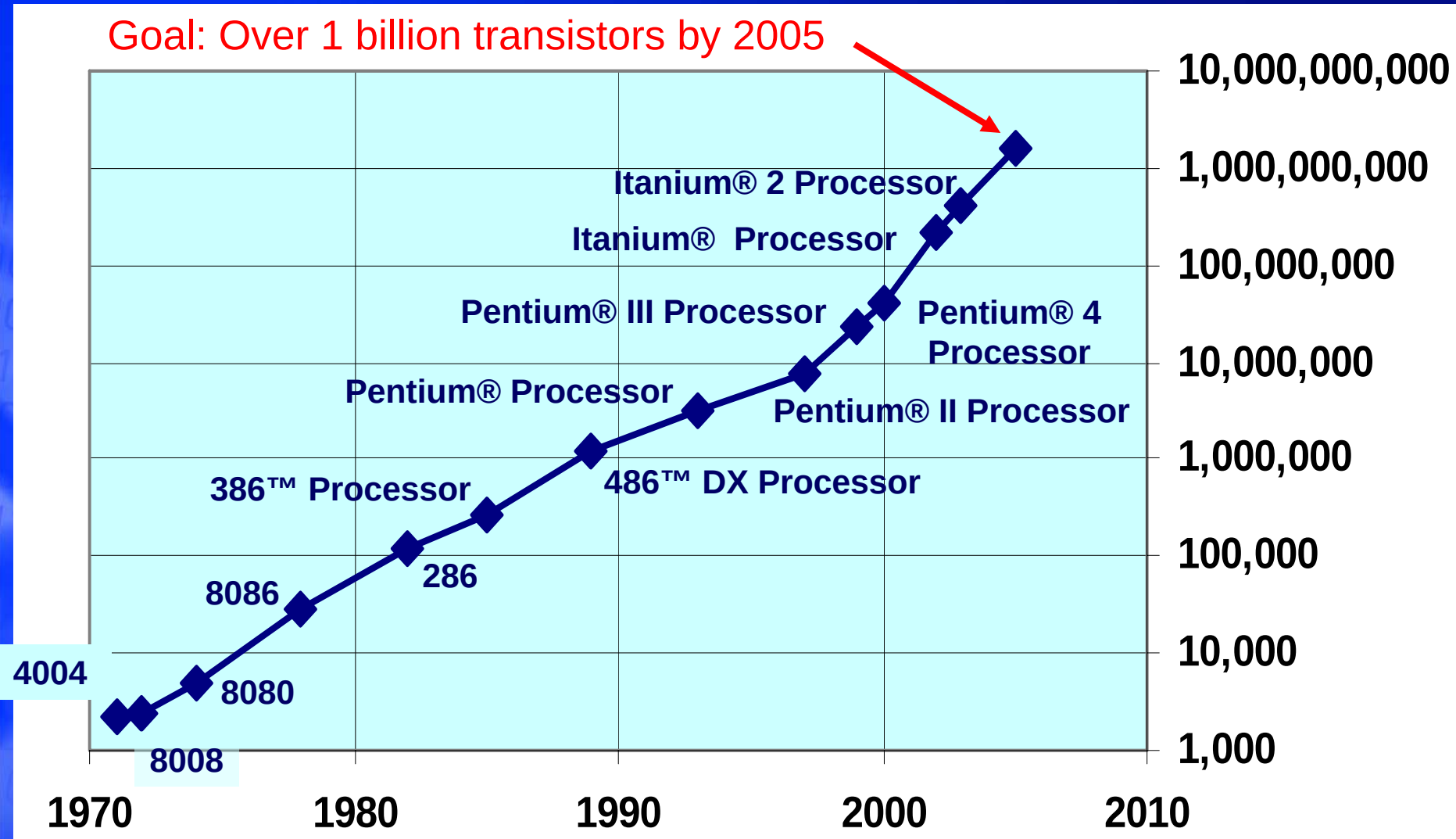
**Gate dielectric thickness = 1.2nm**

# Nanotechnology

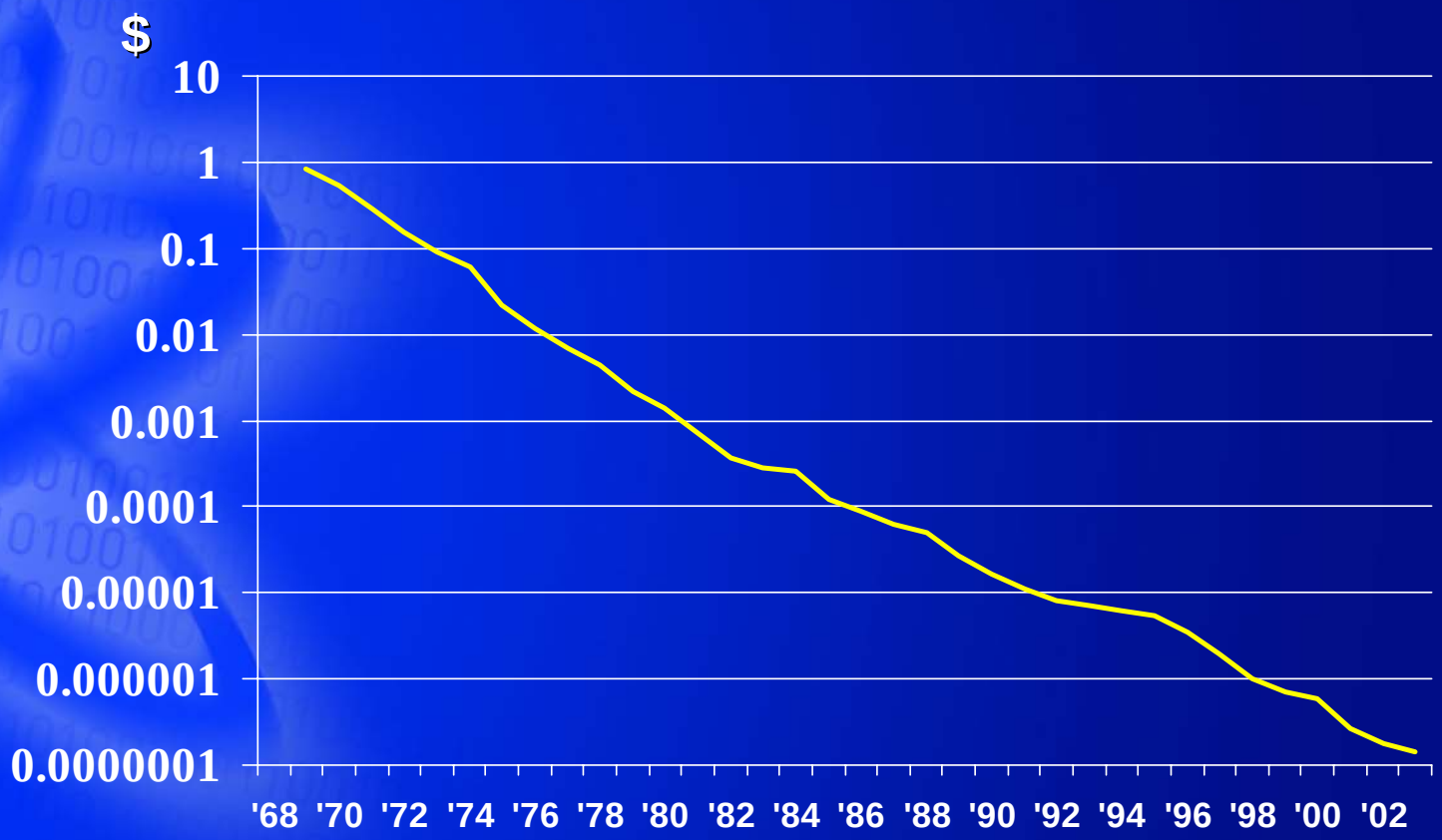
***"Working at the atomic, molecular and supramolecular levels, in the length scale of approximately 1 – 100 nm range, in order to understand and create materials, devices and systems with fundamentally new properties and functions because of their small structure"-M. Roco, NNI***

**Intel's chip technology has novel properties, because of its functionality is determined by its size, and because of specific nanoscale design strategies**

# Moore's Law Continues



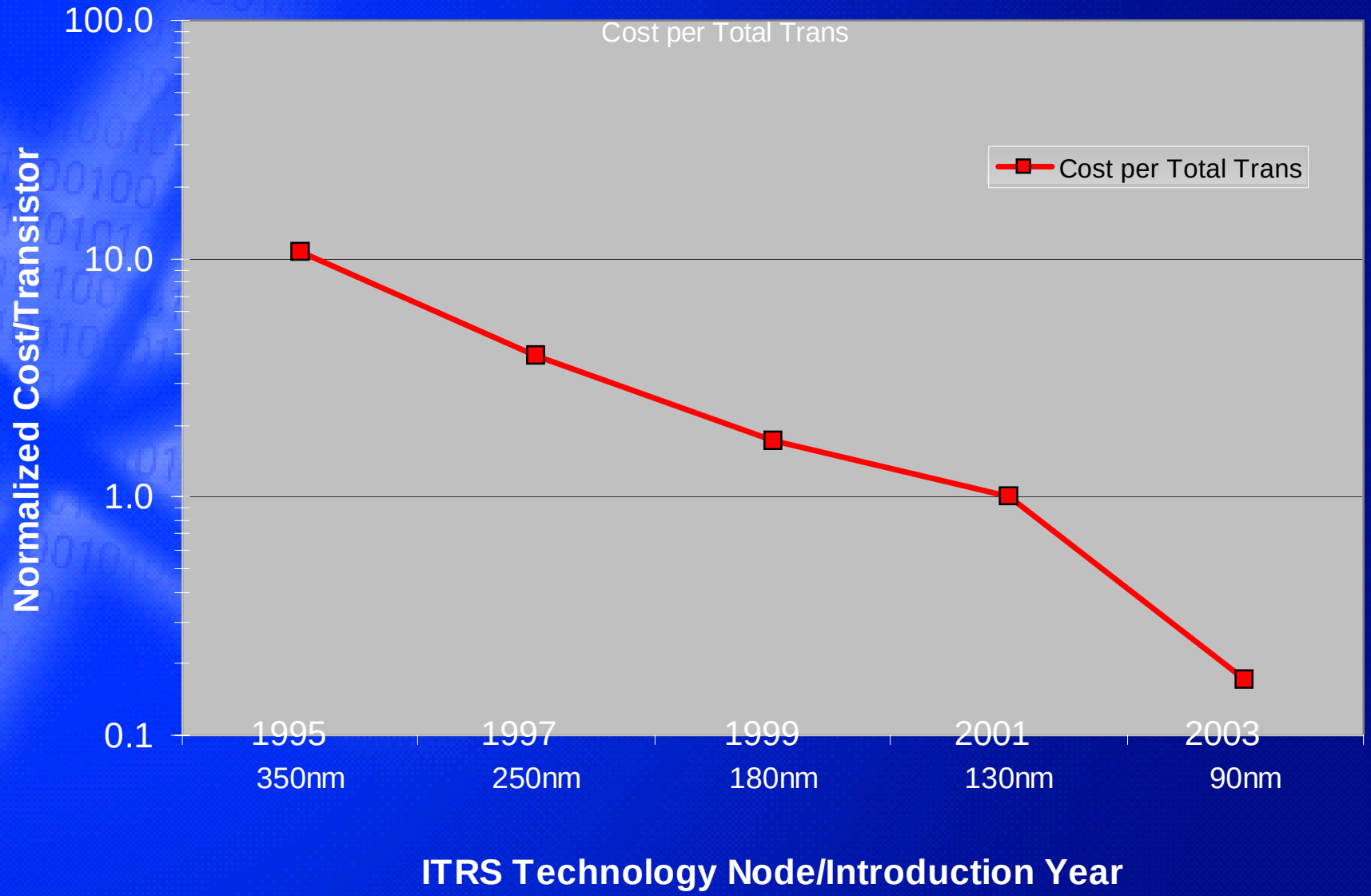
# Average Transistor Price by Year




**There is no "Moore's Second Law"!**

Source: WSTS/Dataquest/Intel, 3/04

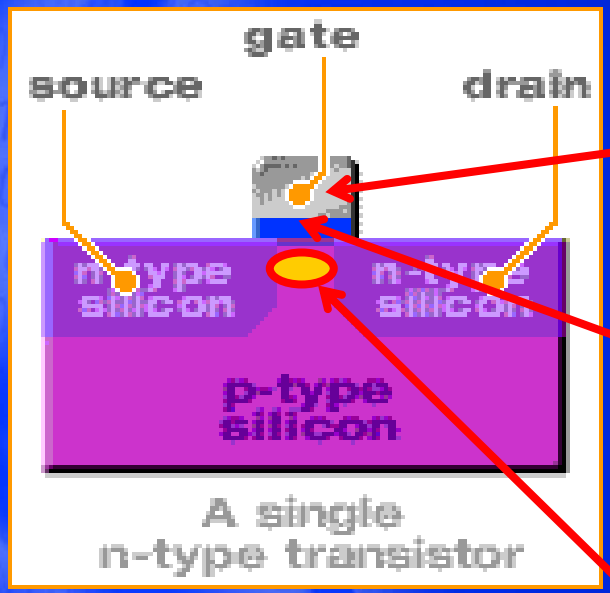
# Cost Trend-No End in Sight

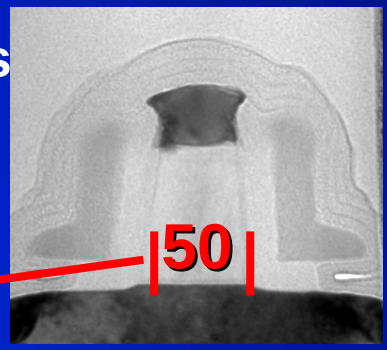


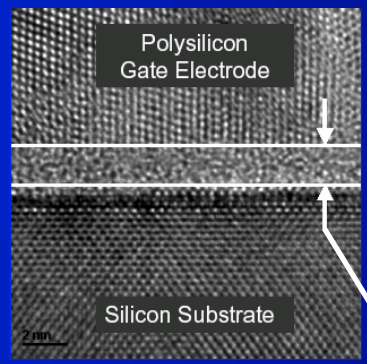

Cost/Transistor Normalized to 130nm Node

# 90 nanometer technology

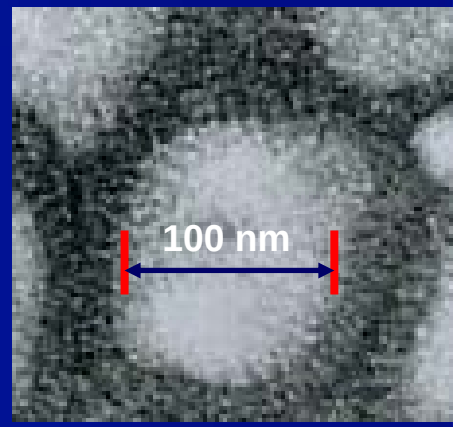
**Nanodesign Strategy - Focus on controlling interfaces and monolayers**
**Surface preparation is key**




**1.2 nm gate oxide is ~5 Silicon atom layers thick!**



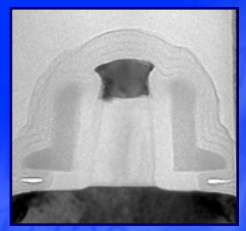

**Influenza virus**

**Source: CDC**

**"Strained Silicon" - Separating the Silicon Atoms for Faster Electron Flow**

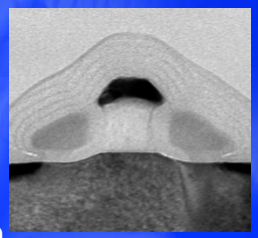
# CMOS Devices Continue

90nm Node
2003



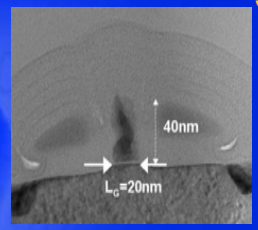
50nm Length
(IEDM2002)

65nm Node
2005



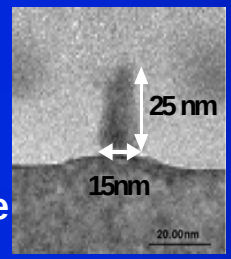
30nm
Prototype
(IEDM2000)

45nm Node
2007



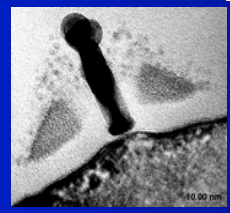

20nm Prototype
(VLSI2001)

32nm Node
2009




15nm Prototype
(IEDM2001)

22nm Node
2011



10nm Prototype
(ITJ 2002)

TMG roadmap
until 2015

1-3nm

16 nm node
2013

7nm

11nm node
2015

5nm

8 nm node
2017

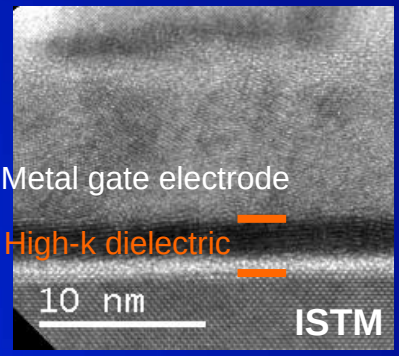
3nm

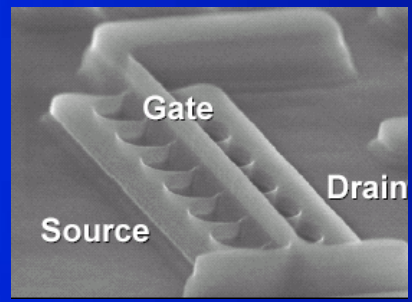
----2003 –2012 ——

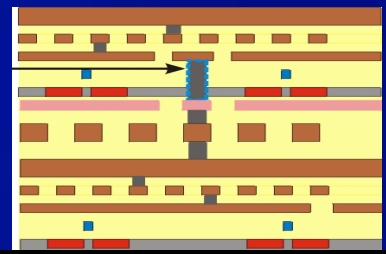
----2013 –2017

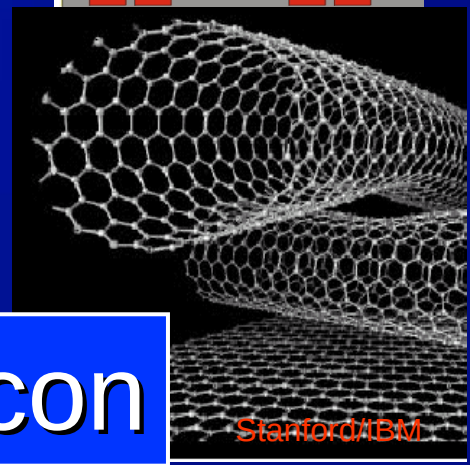
# Scaling

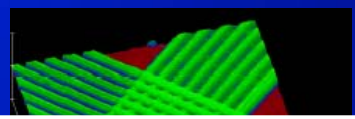
- No fundamental changes in CMOS down to 10nm
  - Expect new
    - materials
    - processes
    - Structures
- Below 10 nm
  - Open minded on options
  - Non-classical CMOS
  - Scalable quantum devices

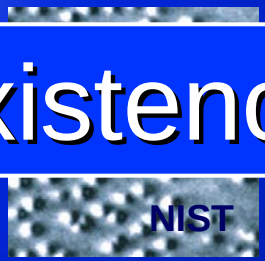




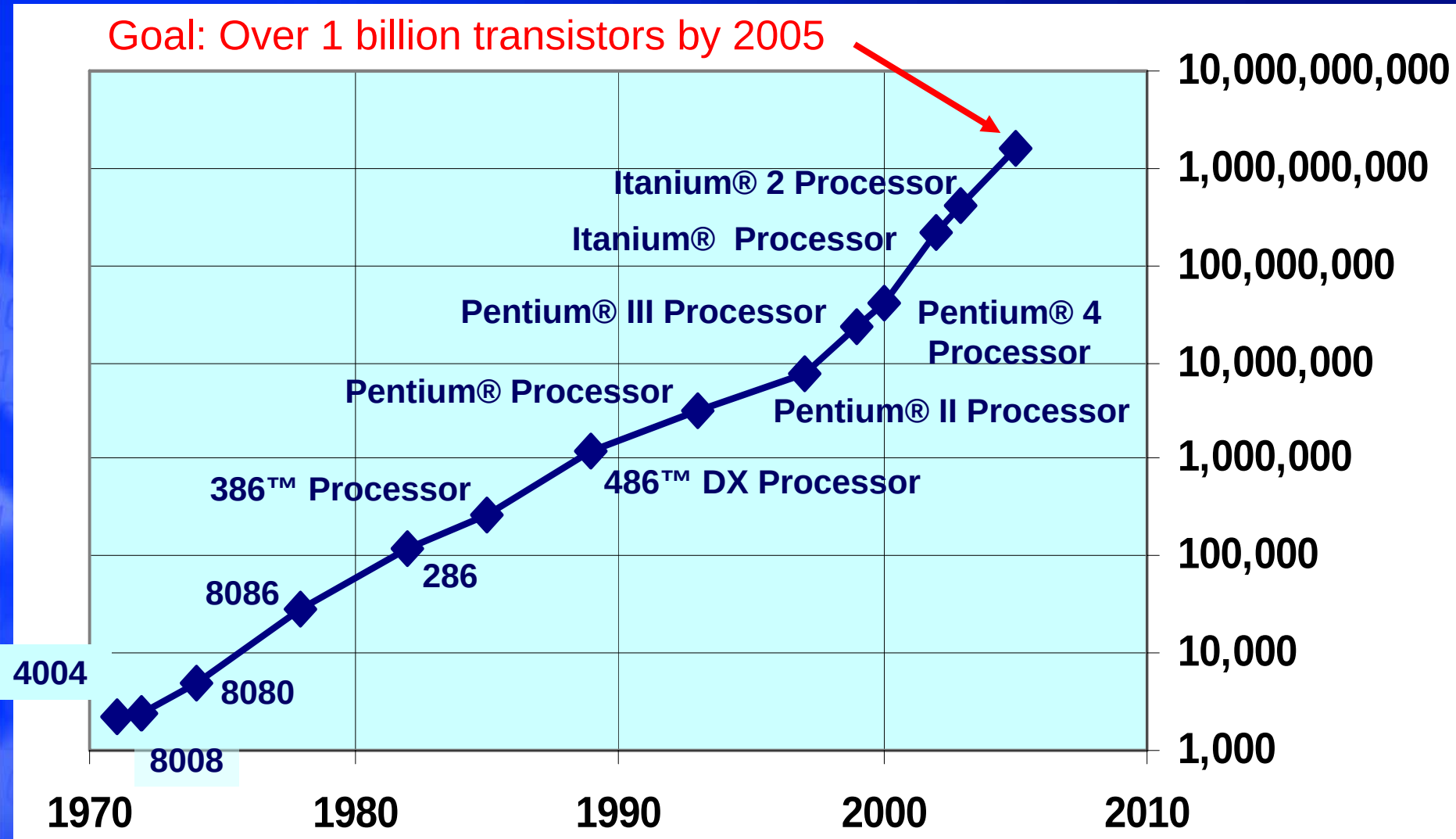





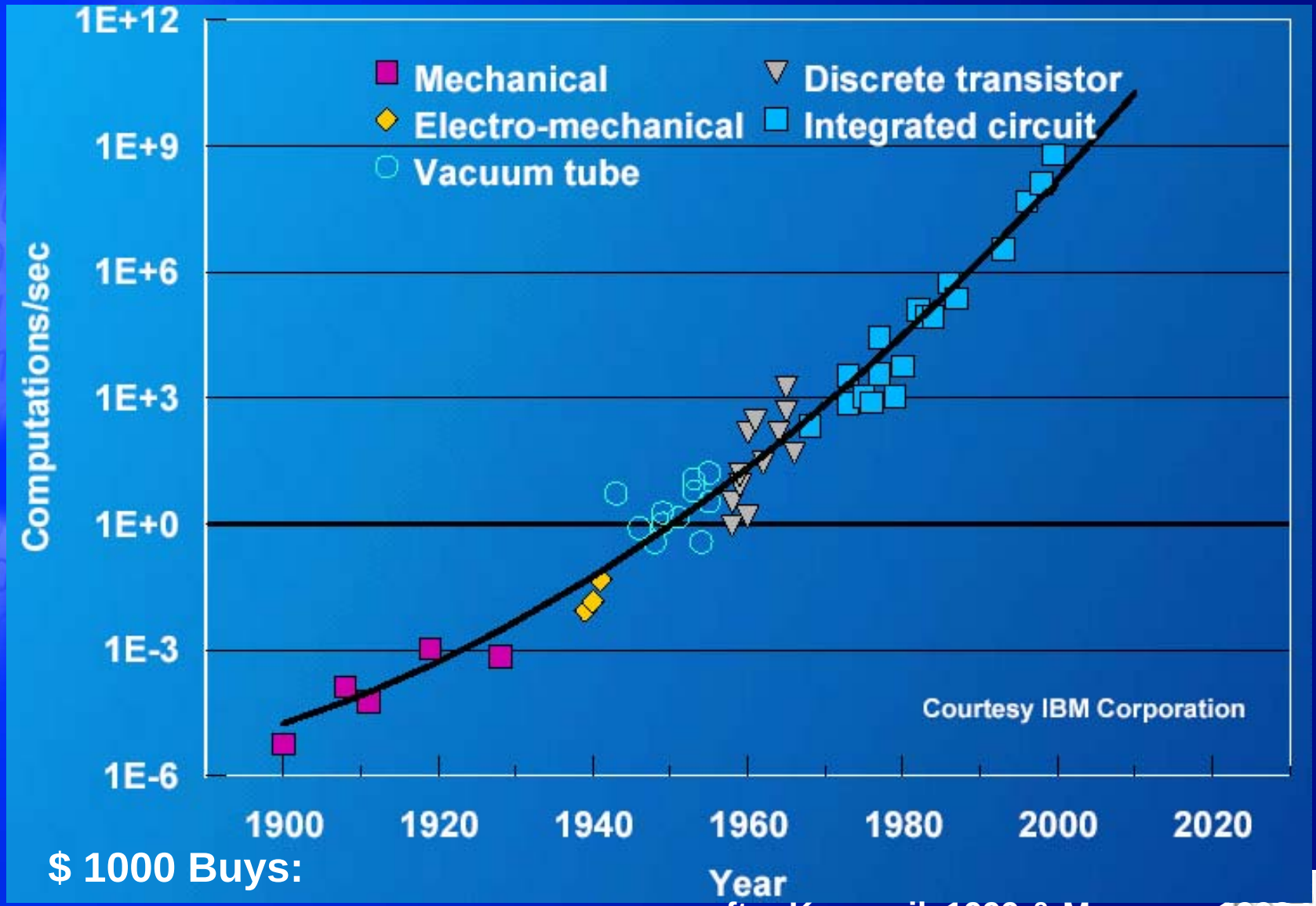


## Co-existence with Silicon

# Moore's Law Continues



# Technology Transitions

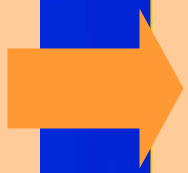



**$ 1000 Buys:**

after Kurzweil, 1999 & Moravec, 1998

# Going Beyond CMOS: Drivers and Approaches

- **Required characteristics:**
  - Scalability
  - Performance
  - Energy efficiency
  - Gain
  - Operational reliability
  - Room temp. operation
- **Preferred approach:**
  - CMOS process compatibility
  - CMOS architectural compatibility



- **Alternative state variables**
  - Spin–electron, nuclear, photon
  - Phase
  - Quantum state
  - Magnetic flux quanta
  - Mechanical deformation
  - Dipole orientation
  - Molecular state
  - …

# Why Nano?

- Semiconductors have a natural synergy between cost and performance
- As semiconductor designs shrink, the cost drops, ***and*** the performance increases

# How will Nano impact your products?

- Product Parameters
  - Function
  - Features
  - Performance
  - Cost
  - Reliability
  - Form factor (size)
- Find the synergies among your product parameters
- Maintain compatibility with existing architectures and infrastructure
- Base milestones on appropriate benchmarks

**Will you find a Moore's Law to drive your technology?**

# Summary

- The semiconductor industry is driven by a “smaller-cheaper-better” model
- Aggressive scaling is an integral part of the semiconductor success story
- There are currently no credible technical or economic arguments that forecast an end to scaling
- Other industries that are entering nanotechnology can learn from the semiconductor industry

# Acknowledgments


- George Bourianoff
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- Jim Hutchby
- Larry Larson
- Jim Meindl
- Frank Robertson
- Peter Zeitzoff
- Victor Zhirnov

A host of researchers whose open literature material is included


For further information on Intel's silicon technology,
please visit the Silicon Showcase at
www.intel.com/research/silicon